

CLAIMS:

1. Contactless integrated circuit (IC1) comprising a device (LMC) for modulating the load of an antenna coil (Ls), a device (CEC1) for extracting a clock (H), and means for delivering a load modulation signal according to a binary signal to be transmitted (DTx), characterized in that it comprises means (CC1) for delivering a pulsed load modulation signal (S1m4) comprising a series of load modulation pulses (I1-In), the duration of which is asynchronously calibrated by the charge or the discharge of at least one capacitor (Cas).

2. Integrated circuit according to claim 1, characterized in that it comprises means (WLCC, INV1, T5, T6) for inhibiting the clock (H) extraction device (CEC1) at least during the emission of the load modulation pulses.

3. Integrated circuit according to one of the claims 1 and 2, wherein the means (CC1) for delivering the pulsed modulation signal (S1m4) comprise at least two capacitors (Cref, Cas) and means (WLCC, CG1, CMP, D6, SR1, T1, T2, T3, T4) for :

- charging the first capacitor (Cref) with a constant current (Iref) before the emission of a load modulation pulse, during a time (Tref) fixed by a predetermined number of clock cycles (H),
- charging the second capacitor (Cas) with a constant current (Iref) during the emission of a pulse, and
- stopping the emission of the pulse when the charge voltage (Vas) of the second capacitor is equal to the voltage (Vref) at the terminals of the first capacitor.

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4. Integrated circuit according to one of the claims 1 to 3, comprising means (WLCC) for :

- transforming the binary signal to be transmitted (DTx) into a binary coded signal (S1) presenting at least, at each bit of the binary signal, a rising or falling variation edge, and
- transforming variation edges of the binary coded signal (S1) into load modulation pulses (I1-In) of short duration compared to the duration (Tb) of a bit of the binary signal to be transmitted (DTx).

5. Integrated circuit according to claim 4, wherein variation edges of a same type only, rising or falling, of the binary coded signal (S1) are transformed into load modulation pulses by the means (CC1) for delivering the pulsed modulation signal.

6. Integrated circuit according to one of the claims 1 to 5, wherein the modulation signal (S1m4) is combined with an a.c. signal (Fsc) in order to form a load modulation signal comprising a.c. signal pulses.

7. Integrated circuit according to one of the claims 1 to 6, wherein the load modulation pulses have a duration (Tas) shorter than or equal to the quarter of the duration of a bit of the binary signal to be transmitted (DTx).

8. Integrated circuit according to one of the claims 1 to 7, wherein the clock extraction device (CEC1) is maintained in an inhibited state after the emission of

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10. Integrated circuit according to one of the claims 1 to 9, characterized in that it comprises means (Pd, C2) for extracting a d.c. supply voltage (Vcc) from the a.c. voltage (Vac) induced in the antenna coil (Ls).

11. Integrated circuit according to one of the claims 1 to 10, wherein the means for inhibiting the clock extraction device (CEC1) comprise means (T5, T6) for powering-off the extraction device (CEC1).